VLSI Design 1: Theory to Tapeout

Summary

ECE 4404/8804 constitutes a comprehensive VLSI design experience for students involving theory, design, verifi- cation and test of a fabricated CMOS digital VLSI design. The centerpiece of this course is a semester-long effort by student-teams to combine basic principles in VLSI design with essential practices and principles that will allow a team of students to produce quality designs productively. Designs built by individual student-teams will be fabricated in an industry standard CMOS process. The fabricated designs will be tested by student-teams to provide hands-on experience with a selection of industry standard test methodologies.

Upon successful completion of this course, students should be able to:

1. Translate the specification of a synchronous digital design into a concise, synthesizable hardware description using System Verilog.
2. Effectively translate large designs from System Verilog into implemented circuits using industry-standard synthesis, place-and-route (SAPR) and verification tools.
3. Appreciate and effectively use best-practices in system building such as trailblazing unknown processes, and develop effective judgement in scoping minimum working examples (MWE) for these efforts.
4. Effectively scope and partition design construction, flow development, validation and test of hardware designs as part of a team effort.
5. Design hardware modules for silicon prototyping and successful testing, characterization and validation.

Lectures

Lectures/live-discussions for this class will be held twice a week at the scheduled time-slots.

Instructors

Primary Instructor: Visvesh Sathe (sathe@gatech.edu)

Instructor office hours: The instructor will plan for two office hours per week. Days TBD

TA office hours: TA assignment for this class is TBD. If one is assigned, TA will offer 4 office hours. If one is not assigned, the instruction will increase office hours to 4 per week. This course also offers “workout” sessions on specific weekends, at critical junctures in the course, to help students make progress on the class toward the tapeout.

Pre-requisites

ECE3150 is the sole prerequisite. Students should be comfortable (or be willing to put in

additional time and effort to be familiar) with basic command-line Linux usage. Basic familiarity with the Verilog Hardware Description Language (HDL) for FPGA implementation will be leveraged in this class.
Familiarity with a scripting language (e.g. Python, Ruby), basic Git repository management, and productive editors (Sublime Text, Vim, Emacs etc.) are a huge design productivity booster and will be very helpful, though not required as prerequisites.

Grading

Students in this course will be graded based on 4 components:

- 8 10-minute quizzes given between week 2 and week 12 in the class. The best 5 quizzes will be considered toward the final grade (10%)
- Individual homework assignments in the first third of the course (10%)
- Team homework assignments given in the second third of the course (10%)
- Course participation, which may take one of several forms: (1) Involvement in lecture; (2) contributing the learning and design quality/productivity of the class on MS Teams (the online communication medium for this class); (3) sharing scripts, methodologies, testbenches to improve outcomes for students. Lasting contributions to the course will be awarded bonus credit per the instructor's discretion. (10%)
- Final project work which includes design review presentations, design quality (correctness, robustness, performance, efficiency) final presentations and a test-chip bringup plan.(50%)

The course is expected to be **very strenuous**. In accordance, grading policy is expected to be liberal. For instance, students with average performance in quizzes and homeworks and a fully functional, verified, robust final project should expect and "A" in this class.

Bonus credits will be offered on multiple occasions to incentivise students to adopt techniques/methodologies and develop valuable industry-relevant skills for improving design quality/productivity. Requiring them, however, constitutes too much effort for the number of credits awarded. Bonus credit will be awarded to provide a potential grade jump to students at the Instructor's discretion.

Homework

Homework in this course will be assigned weekly or every other week (depending on the homework in question). A portion of the assigned homework is to be completed individually while the rest is to be completed as a team. Assignments will take the form of assignments to allow students to build a firm grasp of (1) Verilog description and verification; (2) Design Synthesis, Place-and-Route techniques; and (3) build and verify modules which will be incorporated into each of their final test-chip designs.

Students will find that homework is not limited to reinforcing the theory taught during lectures, as is typical of most courses. Instead homework will cover material which requires an understanding of some of the theory covered in class, but include additional components intended for hands-on learning. **IC design is a practitioner's art**. Consequently, homework is not solely designed to facilitate mastering VLSI theory. Instead, homework is built to ***complement*** the theory taught in class to allow students to build hands-on techniques that are difficult to teach in a classroom setting. To complete these homework assignments, students will synthesize their (1) understanding of the theory covered in class together with; (2) an ability to look through provided design and tooling documentation together with (3) skills they will develop to effectively manage multiple designs, files, and tools to produce robust, functional designs.

The homework assignments in this class are staged to grow in scale and complexity to ramp student-teams up to project completion.

Course Materials

Assignments, references, tutorials, lecture notes will be made available on Canvas. Students will submit their homework by placing their design and README files in assignment-designated directories.

Lecture videos will be recorded and provided. Because of the initial offerings of this class, and the technology-sensitive nature of some of it's content, the portal for viewing lecture material is TBD.

On-line communications will be conducted through MS-Teams. This communication will include announcements and Q&A. It is also intended to facilitate student-team communication during the course. *Please install and try out MS teams ahead of time if possible*

References: There are no required references for this class. Lecture notes, and reading assignments will be sufficient to understand the theoretical material I will cover in this class. Students who would like additional VLSI references can refer to the excellent and simply-written book by Weste and Harris or a more circuit-oriented book by Rabaey et al.

Course Expectations and Guidelines

Academic integrity

Georgia Tech aims to cultivate a community based on trust, academic integrity, and honor. It is expected that students will act in accordance with the highest ethical standards. Information on Georgia Tech's Academic Honor Code can be found here. Students suspected of cheating or plagiarizing on a quiz, exam, or assignment will be reported to the Office of Student Integrity without exception. The office will investigate the incident and identify the appropriate penalty for violations. **Distribution/Sharing course materials and/or using external sites for assistance (e.g., contributing to test banks, CourseHero, Chegg, or similar sites) is prohibited.**

Collaboration and group work

Students are **strongly** encouraged to discuss homework problem strategies and related concepts with one another. However, each student must formulate and turn in their own solutions written in their own words. Cases where scripts, programs, design descriptions, or any relevant material appear to be identical or nearly identical will be immediately referred to the Office of Student Integrity.

Use of Generative AI tools

We welcome the use of generative AI tools in design. Please post on the Teams channel, any and all strategies that allow you to produce/verify/analyze your designs more effectively, do better in quizzes, or better help you organize your tapeout effort. We look to you to trailblaze this promising new way of doing work. **However**, when you use AI, please clearly cite the use of the technology in any written or verbal report – there will be no loss of credit for using AI in any way. Also, use this technology at your own risk – no special consideration will be given to errors arising from use of Gen.AI, unless explicitly agreed upon with the Instructor on a specific body of work.

Absences, late assignments, and missed quizzes

Active participation in the class discussions is a factor in your grade. Attendance of lecture sessions is, however, **optional**. Please note that because quizzes are held at the beginning of some lecture sessions, students who want to give the quiz but not attend the lecture are free to leave without any prejudice whatsoever. While your instructor would love, appreciate and try to elicit spirited discussion during lectures, it is appreciated that not all students will be comfortable with such a form of contribution. Students may contribute in other substantive ways, including sharing scripts, methodologies, answering questions posed by other students on MS teams etc.

As students in this course will hopefully eventually appreciate, homeworks constitute key checkpoints that contribute toward the timely construction of a quality design that will eventually be successfully tested. Maintaining a regular cadence toward project completion is critical. Submitting a late homework steals time from the next milestone, making it harder to meet, and so on until the executing the final project becomes un-viable. To actively avoid such a situation, late homeworks will be aggressively penalized with the intent of avoid your project spiralling out of control, and not serving as a punitive grade-discrimination mechanism.

Accommodations for students with disabilities

If you are a student with learning needs that require special accommodation, contact the Office of Disability Services at (404)894-2563 or disabilityservices.gatech.edu, as soon as possible, to make an appointment to discuss your special needs and to obtain an accommodations letter. Please also e-mail me as soon as possible in order to set up a time to

discuss your learning needs.

Student-Faculty expectations agreement It is important to strive for a atmosphere of mutual respect and responsibility between faculty members and students. In the end, a respect for knowledge and understanding, an appreciation for hard work, and respectful interactions all contribute to an environment conducive to learning and excellence. I encourage you to remain committed to the ideals of Georgia Tech while in this class. See www.catalog.gatech.edu/rules/22 for a description of some basic expectations that we can have of each other.

Outline

The outline below is to be treated as an approximation. Since this is the first offering of this class, and my first offering at Georgia Tech., some run-time adjustments will be inevitable.

1. Timing analysis for flip-flops and latches – a designers perspective.
2. Pipelining and parallel processing.
3. Synthesis, Auto-place and Route – a designer's perspective.
4. Memories (SRAM, DRAM, ROM) – a designer's perspective.
5. Design construction strategies (trailblazing, minimum working examples).
6. System Verilog overview.
7. Logical and physical interconnect (wires, buses).
8. Basic Verification methodologies and techniques (Formal Verification is **not** currently included).
9. Crossing clock and voltage domains (FIFOs metastability and synchronization).
10. Robustly Resetting large digital systems - the basics.
11. Design for Test (BIST, Scan).
12. Design for Manufacturibility (EM, IR).
13. Clock generation and distribution basics (PLLs, DLLs, distribution structures).
14. Process, Voltage and Temperature Variability (OCV, AOCV)