ECE 8803 ALT Advanced Logic Transistor: Physics and Technology (Spring 2023)

Unit: 3

Time: Mon, Wed 1400-1515

Location: 2456 Klaus Advanced Computing

Instructor: Dr. Suman Datta, *Joseph M Pettit Chair in Advanced Computing and Professor of Electrical and Computer Engineering, Georgia Institute of Technology*

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Course Objectives:

To develop fundamental understanding of scattering limited transport versus ballistic transport of carriers in modern semiconductor devices, to quantitively analyze the electrostatic robustness in ultra-scaled MOS transistors and to introduce graduate students specializing in semiconductor science and technology to the process of identifying the mechanisms which limit the modern-day transistor performance, both intrinsic and extrinsic, and seed new ideas for future improvement of transistors from the standpoint of scaling, performance and energy efficiency.

Prospective Students:

Graduate students in electrical and computer engineering program as well as in materials science and engineering program are welcome to take the course. Students majoring in TIGs of nanotechnology and VLSI systems and digital design who are interested in the physics and technology of advanced CMOS logic will be interested in taking this course to get acquainted with the state-of-the-art. The course content emphasizes not only the foundational principles of MOSFETs but also highlights salient features of technologies like FinFETs and Nanosheet FETs; thus, the students are expected to actively read literature as part of the learning process.

Course Outcomes

Upon successful completion of this course, students should be able to:

- analyze the ballistic efficiency in modern-day FinFETs
- analyze the intrinsic and extrinsic factors that limit current and future MOSFET performance.
- analyze the fundamental trade-offs between speed, leakage, and dynamic power consumption in state-of-the-art CMOS
- analyze the scaling trend of the mainstream high-performance logic technology
- explore new ideas that can improve future CMOS transistor technology
- quantitatively evaluate energy-delay metrics of various competing future candidates for high-performance and energy-efficient logic

Prerequisites

Undergraduate-level knowledge about semiconductor devices are required.

Assignments and Grading:

Homework 50%, 5 problem sets (10% each). Pre-knowledge about numerical tools such as MATLAB is required.

Midterm Exam (Mid-semester) 25%, Open book and Open lecture notes, one cheat sheet and a calculator allowed.

Final Exam (Final Exam Period) 25%. Open book and Open lecture notes, one cheat sheet and a calculator allowed.

Expected grade distribution: 85+ is A, 70+ is B, 55+ is C, 40+ is D, <40 is F.

No official textbook required, optional references are

1. S. Datta "Electronic Transport in Mesoscopic Systems",
2. Mark Lundstrom and Jing Guo "Nanoscale Transistors: Device Physics, Modeling and Simulation" Published by Springer.

Notes/ Policy

- If you turn in your homework after the deadline, your score will be multiplied by a factor of 80% for one day late, 50% for two days late, and no score beyond three days late.
- Submit homework in the electronically scanned version.
- Questions regarding homework/exam grading must be asked within one week after the homework/exam is returned.

Academic Honor Code

The Honor Code applies to every aspect of this class, with only one noteworthy exception: student discussion of concepts and techniques for solving homework problems is permitted outside the classroom. However, all the submitted work must be original and by individual. More details on academic honor code can be found at http://www.policylibrary.gatech.edu/student-affairs/academic-honor-code

Access and Accommodations

At Georgia Tech we strive to make learning experiences as accessible as possible. If you anticipate or experience physical or academic barriers based on disability, you are welcome to let me know so that we can discuss options. You are also encouraged to contact the Office of Disability Services to explore reasonable accommodations. More details can be found at https://disabilityservices.gatech.edu/

Absence Policy

The class will follow the Institute absence policy detailed at
http://www.catalog.gatech.edu/rules/4/

Student-Faculty Expectations Agreement

At Georgia Tech we believe that it is important to strive for an atmosphere of mutual respect, acknowledgement, and responsibility between faculty members and the student body. See http://www.catalog.gatech.edu/rules/22/

Course Outline

a) Electron dynamics
- Landauer Transport Equation
- Boltzmann Transport Equation (BTE)
- Solving the BTE in equilibrium
- Evaluating moments of the distribution function

b) Off-equilibrium transport in devices
- Simplified approximations to carrier distribution function (displaced Maxwellian)
- Energy relaxation mechanisms

c) Ballistic and quantum ballistic transport
- Solving the ballistic BTE
- Resistance of a ballistic conductor
- Quasi-ballistic transport
- Examples: ultra-short channel MOSFET, quantum well FET, cryogenic MOSFET

d) Collision-dominated transport
- Relaxation time approximation
- Carrier scattering in bulk and in low-dimensional systems
- Low-field mobility, conductivity mass tensor
- High-field transport
- Monte Carlo simulation of transport

e) Extremely scaled MOSFETs
- Scaling theory
- Virtual source model: above and below threshold
- Virtual source model: quasi ballistic and ballistic
- Leakage
- Parasitic Resistance and Capacitance
- Variation
- Reliability

f) Projects assigned to students to analyze nanoscale devices (e.g 10nm node commercial FinFETs)