ECE 8803 Memory Device Technologies and Applications

3-0-0-3

Time: TBD

Location: TBD

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Detailed Course Description:

The functionality and performance of today's computer system is increasingly dependent on the characteristics of the memory components. This course covers the semiconductor memory technologies from the device bit-cell structures to the memory array design with an emphasis on the industry trend and cutting-edge technologies. The first part of the course discusses the mainstream semiconductor memory technologies that enable various levels in the memory hierarchy, including SRAM, DRAM, and NAND FLASH. Issues such as basic operation principles, device physics, manufacturing processes, bit-cell design considerations, array architectures and technology scaling trends will be discussed. The second part of the course discusses the emerging memory candidates that may have the potential to change the memory hierarchy, including MRAM, PCM, RRAM and FeFET/FeRAM, as well as their new applications beyond the conventional applications, including reconfigurable logic, non-volatile logic, compute-in-memory, deep learning accelerators.

Prospective Students:

Historically, the ECE curriculum emphasizes the logic components, e.g., the transistor technology at the device level or the microprocessor design at the architecture level. This course covers the overlooked part - the memory components, with a holistic view from the device level to the array level. Therefore, the students focusing on nanotechnology, VLSI systems and digital design may be interested in taking this course to broaden their skills and vision. The course is a cutting-edge technology-oriented course, thus the students are expected to actively read the related literature as part of the learning process.

Course Objectives

As part of this course, students

- analyze the operations of a semiconductor memory bit-cell and its related stability, variability and reliability issues.
- analyze the operations of a memory array with peripheral circuitry with appropriate read/write timing and biases.
- analyze the scaling trend of the mainstream memory technologies.
- explore the new applications for the emerging memory technologies.
- utilize the design automation software tools to optimize the memory-bit cell and peripheral circuitry design.

Learning Outcomes

Upon successful completion of this course, students should be able to

- Analyze and design of basic memory bit-cells including 6-transistor SRAM, 1-transistor-1-capacitor DRAM, and floating-gate FLASH transistor.
- Analyze and design of the peripheral circuits including the sense amplifier and array-level organization for the memory array.
- Understand the industry trend of the memory technologies such as FinFET based SRAM, 3D TSV based HBM, 3D NAND, and 3D X-point array.
- Assess the pros and cons of emerging memory technologies such as STT-MRAM, PCM, RRAM and FeFET compared to the mainstream technologies.

Prerequisites

Undergraduate-level semiconductor device physics and digital integrated circuit design courses are strongly advised, e.g., ECE3040 Microelectronic Circuits, ECE3150 VLSI and Advanced Digital Design, or equivalents.

Assignments and Grading:

Homework 50%, 5 problem sets (10% each). Pre-knowledge about numerical tools such as MATLAB is required.

Midterm Exam25%, Close book and close lecture notes, one cheat sheet and a calculator allowed.

Final Exam 25%. Close book and close lecture notes, one cheat sheet and a calculator allowed.

Expected grade distribution: 85+ is A, 70+ is B, 55+ is C, 40+ is D, <40 is F.

No official textbook required; optional references are:

1. Low Power and Reliable SRAM Memory Cell and Array Design, Authors: Koichiro Ishibashi, Kenichi Osada, Publisher: Springer, 2011.
2. DRAM Circuit Design: Fundamental and High-Speed Topics, 2nd edition, Authors: Brent Keeth, R. Jacob Baker, Brian Johnson, Feng Lin, Publisher: John Wiley & Sons, 2008.
3. NAND FLASH Memory Technologies, Author: Seiichi Aritome, Publisher: Wiley-IEEE Press, 2016.

Notes/ Policy
- If you miss an exam without an approved absence (see Absence Policy below), you will get a zero.
- If you turn in your homework after the deadline, your score will be multiplied by a factor of 80% for one day late, 50% for two days late, and no score beyond three days late.
- Submit homework in the electronic scanned version.
- Questions regarding homework/exam grading must be asked within one week after the homework/exam is returned.

Academic Honor Code

The Honor Code applies to every aspect of this class, with only one noteworthy exception: student discussion of concepts and techniques for solving homework problems or lab projects is permitted outside the classroom. However, all the submitted work must be original and by individual. More details on academic honor code can be found at
http://www.policylibrary.gatech.edu/student-affairs/academic-honor-code

Access and Accommodations

At Georgia Tech we strive to make learning experiences as accessible as possible. If you anticipate or experience physical or academic barriers based on disability, you are welcome to let me know so that we can discuss options. You are also encouraged to contact the Office of Disability Services to explore reasonable accommodations. More details can be found at
https://disabilityservices.gatech.edu/

Absence Policy

The class will follow the Institute absence policy detailed at
http://www.catalog.gatech.edu/rules/4/

Course Outline

- **Semiconductor Memory and CMOS Scaling Overview**
  - Introduction, industry trend, technology scaling
- **SRAM**
  - 6T cell operation
  - Noise margin, stability, scaling issues, and layout
  - Variability and reliability issues
  - Recent trends: FinFET
- **DRAM**
  - 1T-1C cell operation
  - Fabrication technology, capacitor structure, and layout
  - Recent trends: 3D TSV based HBM
- **FLASH memory**

- FLASH device physics
- NAND vs. NOR architecture
- Reliability and scaling issues
- Recent trends: 3D vertical NAND

- **Emerging memories**
  - Cross-point array architecture (3D X-point)
  - RRAM
  - PCM
  - STT-MRAM/SOT-MRAM
  - FeFET/FeRAM
- **Memory Array Design**
  - Peripheral circuits
  - Sense amplifier design
  - NVSim simulator
- **New applications**
  - Non-volatile cache
  - Reconfigurable logic
  - In-memory computing for deep learning